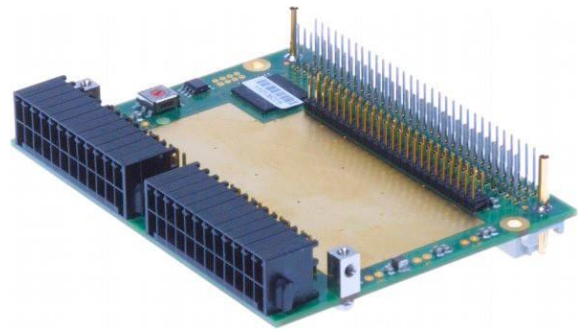


32. COP-Proto-S6 (Prototype Board)

COP-Proto-S6

611143700

The COP-Proto-S6 is a prototype board which, starting from the Spartan 6 FPGA employed, provides a total of 48 IOs. It enables the customer to develop and simply integrate its own specific interfaces into the Intel system. The IOs can be configured in the software as an input or output and operated up to 16kHz via COP bus.



32.1. Technical Specifications

IOs		
Number IOs	48	
COP bus sampling rate	16	kHz
Outputs		
Technology	3.3V CMOS	
Maximum output low level	0.4	V
Maximum output high level	2.9	V
Maximum output current	15	mA
Capacity	10	pF
Pull-up	approx. 10	kΩ
Inputs		
Technology	3.3V CMOS	
Input voltage Vmin	-0.4	V
Input voltage Vmax	4.1	V
Low input threshold	< 0.8	V
High input threshold	> 2	V
Capacity	10	pF
Pull-up	Approx. 10	kΩ
Module		
Maximum power consumption at 24V node power supply	100	mA

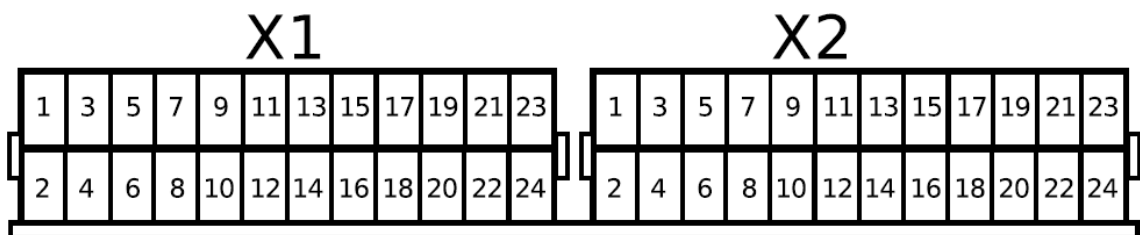
32.2. Use and Warranty

The COP-Proto-S6 is delivered with pre-assembled pin strips. The customer must build its prototypes so that the module could be tested and repaired without any customer-specific peripherals having to be connected to it, for example, by using an add-on board. Any modules received in a state other than the delivery one has neither been tested nor repaired by Indel.



Since the FPGA can be destroyed when improperly handled, it is not covered by the warranty. In general, Indel recommends using appropriate drivers for the protection of FPGAs.

32.3. Pin Assignment



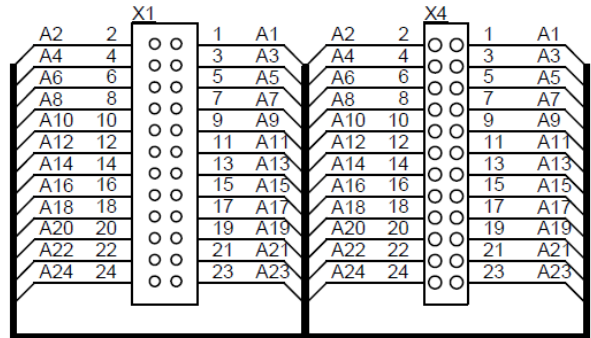
X1					
No.	Dir	Id.	Id.	Dir	No.
2		A2	A1		1
4		A4	A3		3
6		A6	A5		5
8		A8	A7		7
10		A10	A9		9
12		A12	A11		11
14		A14	A13		13
16		A16	A15		15
18		A18	A17		17
20		A20	A19		19
22		A22	A21		21
24		A24	A23		23

X2					
No.	Dir	Id.	Id.	Dir	No.
2		B2	B1		1
4		B4	B3		3
6		B6	B5		5
8		B8	B7		7
10		B10	B9		9
12		B12	B11		11
14		B14	B13		13
16		B16	B15		15
18		B18	B17		17
20		B20	B19		19
22		B22	B21		21
24		B24	B23		23

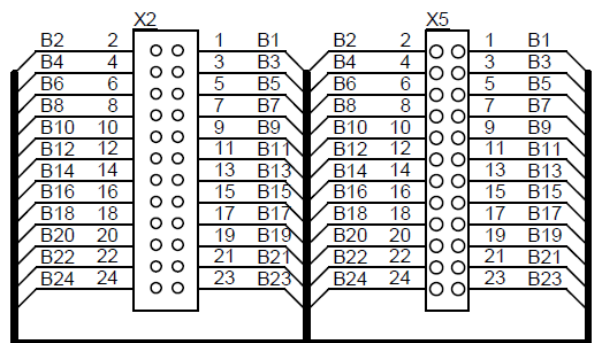
32.4. **Diagram**

Pin strips

Connector terminals X1 are reproduced one-to-one on connector strip X4 in a 2.54mm grid.

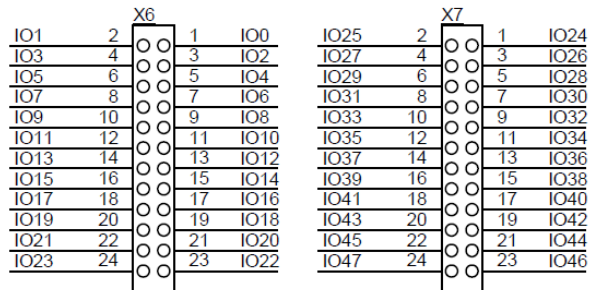


Connector terminals X2 are reproduced one-to-one on connector strip X5 in a 2.54mm grid.



FPGA IOs

The IOs from FPGA are also reproduced on connector strips in a 2.54mm grid. Each 2x12 connector strip has 24 IOs.



32.5. **Available Options**

Item Number	Label	Option	Description
611143700	COP-Proto-S6		Spartan 6 prototype board 48 IOs from FPGA, 3.3V CMOS, 2 x 24-pole connectors for Wago female connectors